# Introduction of a typical module lead resistance and chip-related on-state characteristics in the data sheets

## Typical module lead resistance

Effective now all data sheets released for new module types will include a value for the lead resistance, meaning the resistive value of the connection between power terminals and chips. With this measure a better utilization of the module as well as a more accurate rating of the thermal design is possible.

Designation : module lead resistance, terminals – chip

Short designation : $R_{CC'+EE'}$
Unit: mΩ

There will be a typical value given for one switch / per arm at 25°C. This is the sum of all ohmic resistances between emitter- and collector-terminals (-pins) and the chips. For modules with several, perhaps different resistances in the separate arms (e.g. sixpacks) the average value of all resistances will be given. The temperature dependency of the module lead resistance is specified by:
$R_{CC'+EE'}(\vartheta) = [1 + \alpha\cdot(\vartheta\text{-}25°C)]\cdot R_{CC'+EE'}(25°C)$ with $\alpha = 3.85\cdot10^{-3}K^{-1}$.

## Chip-related on-state characteristics

Newly released IGBT type ranges, starting with PIM and 600V modules, will be characterized chip-related. In the data sheets the values for $V_{cesat}$ and $V_f$ as well as the corresponding diagrams are affected.
The $R_{thJC}$ is already determined chip-related. The RBSOA diagram will further be given chip- and terminal-related .
The new data sheets (chip-related) can be distinguished from those released up to now (terminal-related) by the existence of the new parameter „module lead resistance“.

Reason for this measure:
The type range of eupec IGBT modules will be continuously expanded to higher currents (at the moment modules with up to 2400A are available) and lower forward voltages (the „low loss“ types). Due to rising current densities the module‘s ohmic resistances of the internal busbars and connections would lead to an increasingly wrong data sheet value for the real chip characteristic if the specification remains terminal-related.

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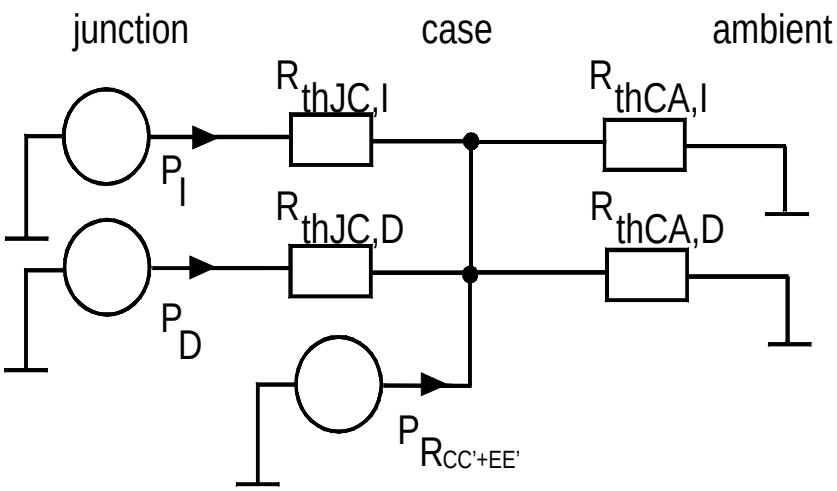
The chip-related data specification of the forward voltages allows a more accurate determination of the junction temperatures by the customer. The parasitic losses caused by the module lead resistance can be determined using the RMS module current.




The thermal equivalent circuit on the left clarifies how device and parasitic losses can be considered in the thermal calculation.

The thermal model shows, that the parasitic losses $P_{v,RCC'+EE'}$ are no longer part of IGBT or diode chip losses, but will be injected directly into the module base plate. They still have to be considered when designing the heat-sink.

The additional cooling effect for the module connected to the main terminals via busbars can be accounted for by an appropriate reduction of the parasitic losses.