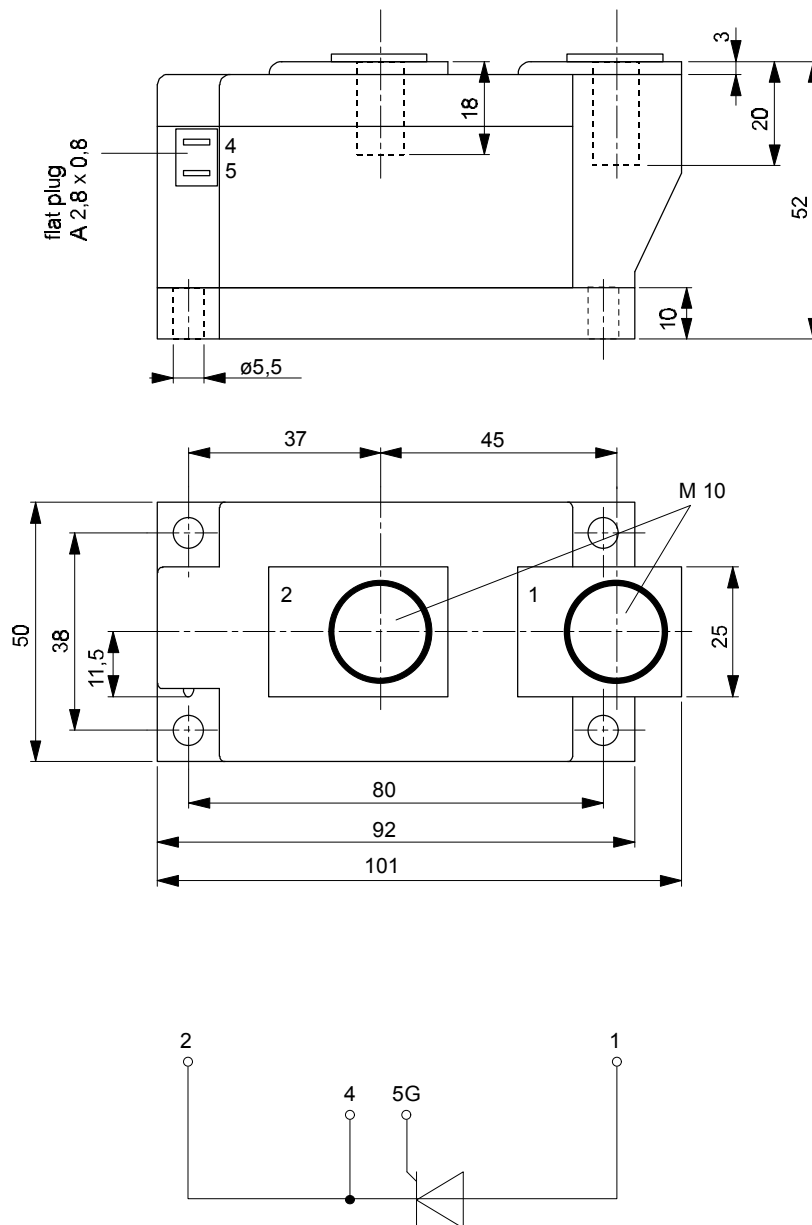




European Power-Semiconductor and Electronics Company

Marketing Information

TZ 335 F



TZ 335 F

Elektrische Eigenschaften	Electrical properties				
Höchstzulässige Werte	Maximum rated values				
Periodische Vorwärts- und Rückwärts-Sperrspannung	repetitive peak forward and reverse voltages	$t_{vj} = -40^{\circ}\text{C} \dots t_{vj \max}$	$V_{\text{DRM}}, V_{\text{RRM}}$	800, 1000, 1100, 1200, 1300	V ¹⁾
Vorwärts-Sperrspannung	non-repetitive peak forward state voltage	$t_{vj} = -40^{\circ}\text{C} \dots t_{vj \max}$	V_{DSM}	800, 1000, 1100, 1200, 1300	V
Rückwärts-Sperrspannung	non-repetitive peak reverse state voltage	$t_{vj} = +25^{\circ}\text{C} \dots t_{vj \max}$	V_{RSM}	900, 1100, 1200, 1300, 1400	V
Durchlaßstrom-Grenzeffektivwert	RMS on-state current		I_{TRMSM}	700	A
Dauergrenzstrom	average on-state current	$t_c = 85^{\circ}\text{C}$	I_{TAVM}	335	A
		$t_c = 68^{\circ}\text{C}$		445	A
Stoßstrom-Grenzwert	surge current	$t_{vj} = 25^{\circ}\text{C}, t_p = 10 \text{ ms}$	I_{TSM}	11,3	kA
		$t_{vj} = t_{vj \max}, t_p = 10 \text{ ms}$		10	kA
Grenzlastintegral	$I^2 t$ -value	$t_{vj} = 25^{\circ}\text{C}, t_p = 10 \text{ ms}$	$I^2 t$	$638 \cdot 10^3$	A ² s
		$t_{vj} = t_{vj \max}, t_p = 10 \text{ ms}$		$500 \cdot 10^3$	A ² s
Kritische Stromsteilheit	critical rate of rise of on-state current	DIN IEC 747-6, f = 50 Hz	$(di_T/dt)_{\text{cr}}$	200	A/μs
		$I_{\text{GM}} = 1 \text{ A}, di_G/dt = 1 \text{ A}/\mu\text{s}$			
Kritische Spannungssteilheit	critical rate of rise of off-state voltage	$t_{vj} = t_{vj \max}, V_D = 0,67 V_{\text{DRM}}$	$(dv_D/dt)_{\text{cr}}$		
		6.Kennbuchstabe/6th letter B		50	50 V/μs
		6.Kennbuchstabe/6th letter C		500	500 V/μs
		6.Kennbuchstabe/6th letter L		500	50 V/μs
		6.Kennbuchstabe/6th letter M		1000	500 V/μs
Charakteristische Werte	Characteristic values				
Durchlaßspannung	on-state voltage	$t_{vj} = t_{vj \max}, I_T = 1300 \text{ A}$	V_T	max.	1,85 V
Schleusenspannung	threshold voltage	$t_{vj} = t_{vj \max}$	$V_{T(\text{TO})}$		1,15 V
Ersatzwiderstand	slope resistance	$t_{vj} = t_{vj \max}$	r_T		0,42 mΩ
Zündstrom	gate trigger current	$t_{vj} = 25^{\circ}\text{C}, V_D = 12 \text{ V}$	I_{GT}	max.	250 mA
Zündspannung	gate trigger voltage	$t_{vj} = 25^{\circ}\text{C}, V_D = 12 \text{ V}$	V_{GT}	max.	2,2 V
Nicht zündender Steuerstrom	gate non-trigger current	$t_{vj} = t_{vj \max}, V_D = 12 \text{ V}$	I_{GD}	max.	10 mA
		$t_{vj} = t_{vj \max}, V_D = 0,5 V_{\text{DRM}}$		max.	5 mA
Nicht zündende Steuerspannung	gate non-trigger voltage	$t_{vj} = t_{vj \max}, V_D = 0,5 V_{\text{DRM}}$	V_{GD}	max.	0,25 V
Haltestrom	holding current	$t_{vj} = 25^{\circ}\text{C}, V_D = 12 \text{ V}, R_A = 10 \Omega$	I_H	max.	250 mA
Einraststrom	latching current	$t_{vj} = 25^{\circ}\text{C}, V_D = 12 \text{ V}, R_{\text{GK}} > = 10 \Omega$	I_L	max.	1000 mA
		$i_{\text{GM}} = 1 \text{ A}, di_G/dt = 1 \text{ A}/\mu\text{s}, t_g = 20 \mu\text{s}$			
Vorwärts- und Rückwärts-Sperrstrom	forward off-state and reverse current	$t_{vj} = t_{vj \max}$	i_D, i_R	max.	100 mA
		$V_D = V_{\text{DRM}}, V_R = V_{\text{RRM}}$			
Zündverzögerung	gate controlled delay time	DIN IEC 747-6, $t_{vj} = 25^{\circ}\text{C}$	t_{gd}	max.	1,5 μs
		$i_{\text{GM}} = 1 \text{ A}, di_G/dt = 1 \text{ A}/\mu\text{s}$			
Freiwerdzeit	circuit commutated turn-off time	$t_{vj} = t_{vj \max}, I_{\text{TM}} = I_{\text{TAVM}}$	t_q		
		$V_{\text{RM}} = 100 \text{ V}, V_{\text{DM}} = 0,67 V_{\text{DRM}}$			
		$-di_T/dt = 20 \text{ A}/\mu\text{s}$			
		$dv_D/dt = 6.\text{Kennbuchstabe}/6\text{th letter}$			
		5.Kennbuchstabe/5th letter E		max.	20 μs
		5.Kennbuchstabe/5th letter F		max.	25 μs
		5.Kennbuchstabe/5th letter G		max.	30 μs
Isolations-Prüfspannung	insulation test voltage	RMS, f = 50 Hz, 1 min.	V_{ISOL}		3 kV
Thermische Eigenschaften	Thermal properties				
Innerer Wärmewiderstand	thermal resistance, junction to case	pro Modul/per module, $\Theta = 180^{\circ} \sin$	R_{thJC}	max.	0,0800 °C/W
		pro Modul/per module, $\Theta = 180^{\circ} \sin$		max.	0,0765 °C/W
Übergangs-Wärmewiderstand	thermal resistance, case to heatsink	pro Modul/per module	R_{thCK}	max.	0,02 °C/W
Höchstzul. Sperrschichttemperatur	max. junction temperature		$t_{vj \max}$		125 °C
Betriebstemperatur	operating temperature		$t_{c \text{ op}}$		-40...+125 °C
Lagertemperatur	storage temperature		t_{stg}		-40...+130 °C
Mechanische Eigenschaften	Mechanical properties				
Gehäuse, siehe Seite	case, see page				
Si-Elemente mit Druckkontakt	Si-pellet with pressure contact				
Innere Isolation	internal insulation				AIN
Anzugsdrehmoment für mechanische Befestigung	mounting torque	Toleranz/tolerance +/- 15%	M1	5	Nm
Anzugsdrehmoment für elektrische Anschlüsse	terminal connection torque	Toleranz/tolerance +5%/-10%	M2	12	Nm
Gewicht	weight		G	typ.	900 g
Kriechstrecke	creepage distance				15 mm
Schwingfestigkeit	vibration resistance	f = 50 Hz			50 m/s ²

¹⁾ 1300 V auf Anfrage / 1300 V on demand

²⁾ Werte nach DIN IEC 747-6 (ohne vorausgehende Kommutierung) / Values according to DIN IEC 747-6 (without prior commutation)

³⁾ Unmittelbar nach der Freiwerdzeit, vgl. Meßbedingungen für t_q / Immediately after circuit commutated turn-off time, see parameters for t_q .

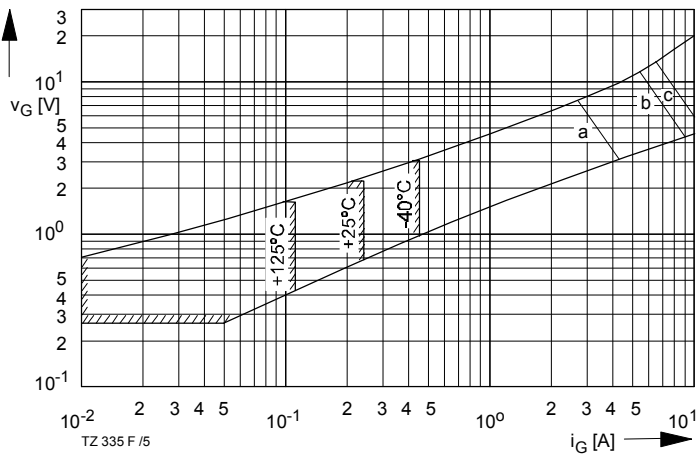


Bild / Fig. 1
 Steuercharakteristik $v_G = f(i_G)$ mit Zündbereich für $V_D = 12V$
 Gate characteristic $v_G = f(i_G)$ with triggering area for $V_D = 12V$
 Höchstzulässige Spitzensteuerverlustleistung / Maximum rated peak gate power dissipation $P_{GM} = f(t_{Gj})$:
 a - 20W/10ms b - 40W/1ms c - 60W/0.5ms

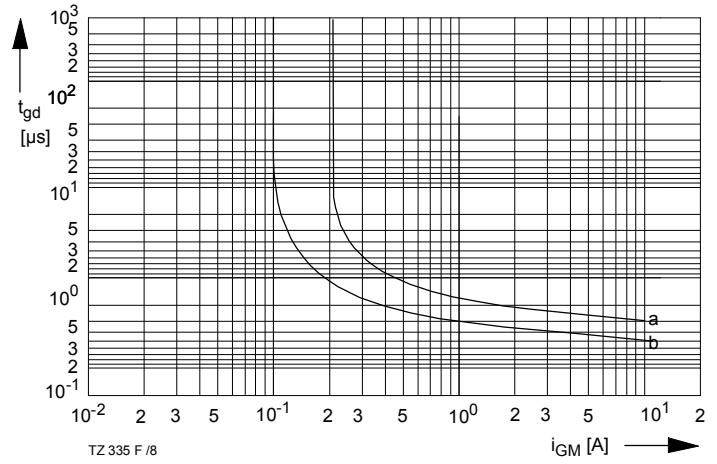


Bild / Fig. 2
 Zündverzug / Gate controlled delay time $t_{gd} = f(i_{GM})$
 $t_{vj} = 25^\circ C, di_G/dt = i_{GM}/1\mu s$
 a - maximaler Verlauf / limiting characteristic
 b - typischer Verlauf / typical characteristic

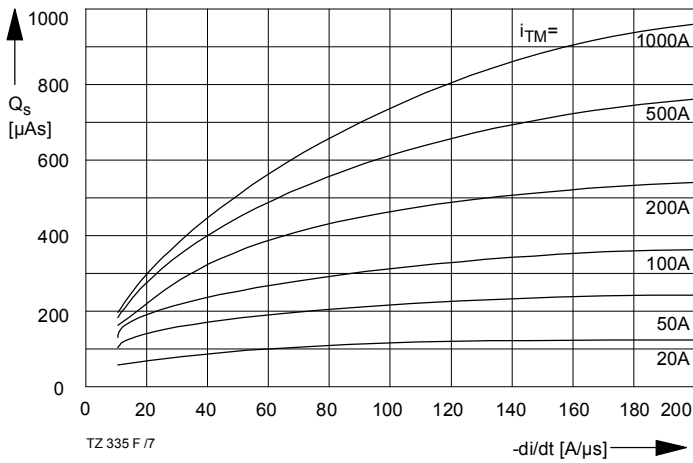


Bild / Fig. 3
 Sperrverzögerungsladung Q_s in Abhängigkeit von der abkommütierenden Stromsteilheit $-di/dt$ bei $t_{vj} = t_{vj\ max}$, $V_R = 0,5 V_{RRM}$, $v_{RM} = 0,8 V_{RRM}$
 Recovered charge Q_s versus the rate of decay of the forward on-state current $-di/dt$ at $t_{vj} = t_{vj\ max}$, $V_R = 0,5 V_{RRM}$, $v_{RM} = 0,8 V_{RRM}$
 Parameter: Durchlaßstrom i_{TM} / On-state current i_{TM}

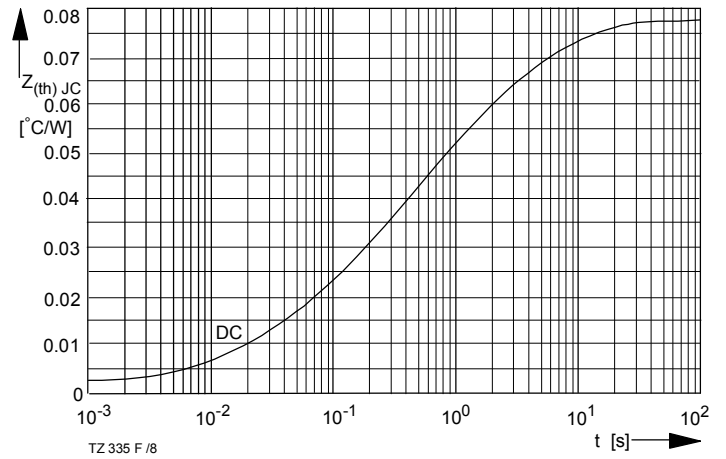


Bild / Fig. 4
 Transienter innerer Wärmewiderstand / Transient thermal impedance $Z_{thJC} = f(t)$

Analytische Elemente des transienten Wärmewiderstandes Z_{thJC} pro Zweig für DC
 Analytical elements of transient thermal impedance Z_{thJC} per arm for DC

Pos. n	1	2	3	4	5	6	7
$R_{thn} [^\circ C/W]$	0,00194	0,00584	0,1465	0,0254	0,0287		
$\tau_n [s]$	0,000732	0,00824	0,108	0,57	3		

Analytische Funktion / Analytical function:

$$Z_{thJC} = \sum_{n=1}^{n_{max}} R_{thn} (1 - e^{-\frac{t}{\tau_n}})$$

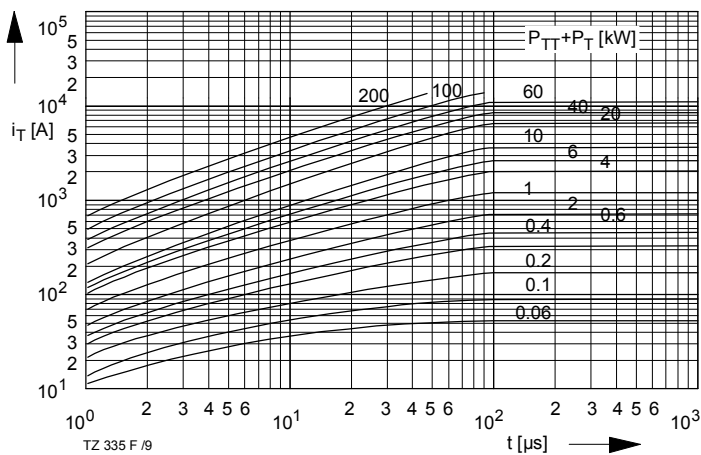


Bild / Fig. 5
 EDL-Diagramm / EDL-diagram

Summe aus Einschalt- und Durchlaßverlustleistung $P_{TT}+P_T$ /
 Sum of the turn-on and on-state power loss $P_{TT}+P_T$

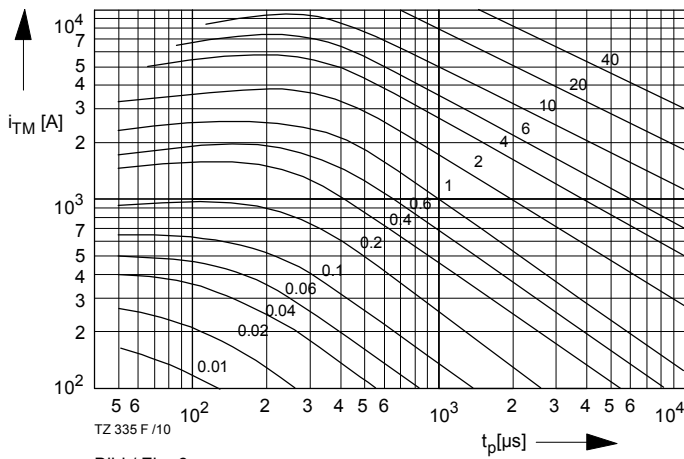
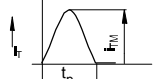
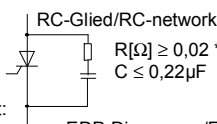


Bild / Fig. 6



Lastkreis / Load circuit:
 $v_{DM} \leq 67\% V_{DRM}$
 $v_{RM} \leq 50V$
 $dv_R/dt \leq 100V/\mu s$



RC-Glied/RC-network:
 $R[\Omega] \geq 0,02 \cdot v_{DM}[V]$
 $C \leq 0,22\mu F$

Steuergenerator /
 Pulse generator:
 $i_G = 1A$
 $di_G/dt = 1A/\mu s$

EDP-Diagramm /EDP-diagram
 Gesamtenergie W_{tot} je Durchlaßstromplus /
 Total energy W_{tot} per on-state current pulse

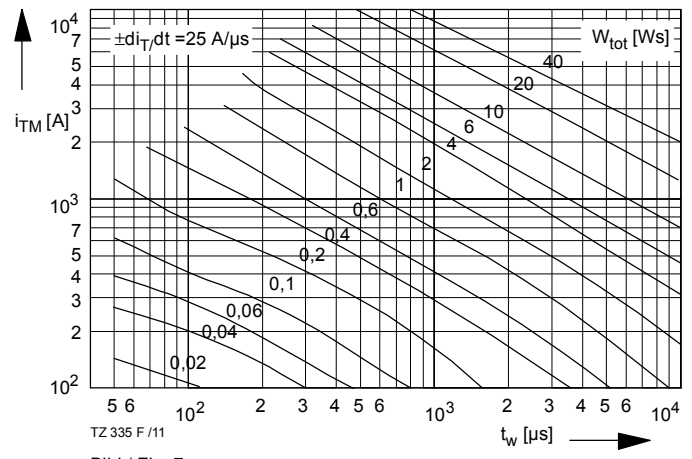
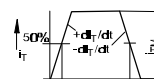
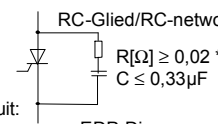


Bild / Fig. 7



Lastkreis / Load circuit:
 $v_{DM} \leq 67\% V_{DRM}$
 $v_{RM} \leq 50V$
 $dv_R/dt \leq 100V/\mu s$



RC-Glied/RC-network:
 $R[\Omega] \geq 0,02 \cdot v_{DM}[V]$
 $C \leq 0,33\mu F$

Steuergenerator /
 Pulse generator:
 $i_G = 1A$
 $di_G/dt = 1A/\mu s$

EDP-Diagramm /EDP-diagram
 Gesamtenergie W_{tot} je Durchlaßstromplus /
 Total energy W_{tot} per on-state current pulse

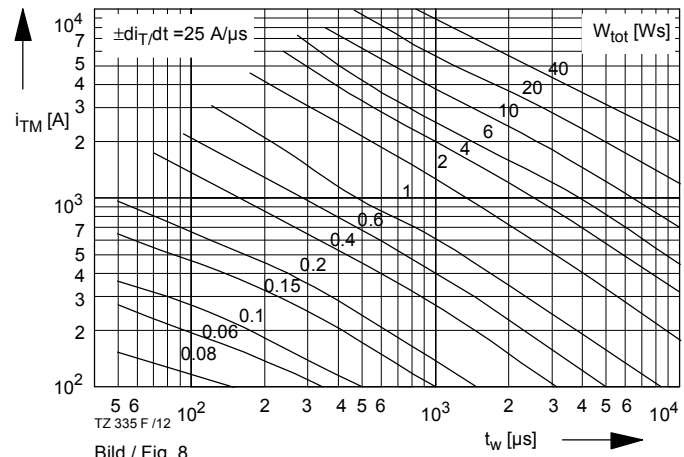
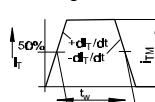
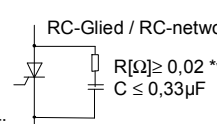


Bild / Fig. 8



Lastkreis / Load circuit:
 $v_{DM} \leq 67\% V_{DRM}$
 $v_{RM} \leq 67\% V_{RRM}$
 $dv_R/dt \leq 600V/\mu s$



RC-Glied / RC-network
 $R[\Omega] \geq 0,02 \cdot v_{DM}[V]$
 $C \leq 0,33\mu F$

Steuergenerator /
 Pulse generator:
 $i_G = 1A$
 $di_G/dt = 1A/\mu s$

EDP-Diagramm /EDP-diagram
 Gesamtenergie W_{tot} je Durchlaßstromplus /
 Total energy W_{tot} per on-state current pulse

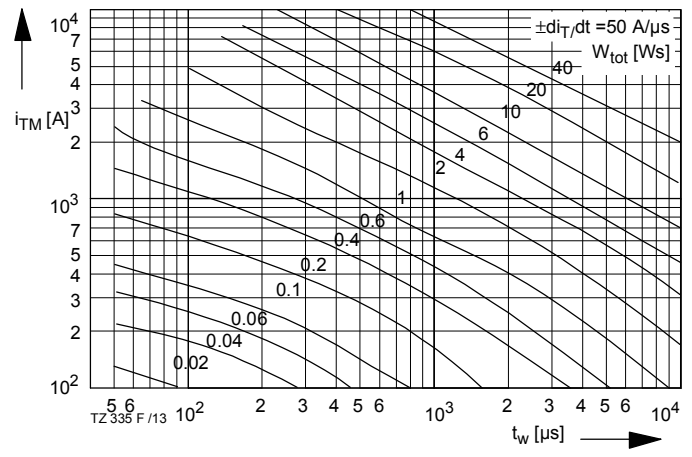
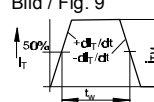
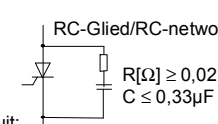


Bild / Fig. 9



Lastkreis / Load circuit:
 $v_{DM} \leq 67\% V_{DRM}$
 $v_{RM} \leq 50V$
 $dv_R/dt \leq 100V/\mu s$



RC-Glied/RC-network:
 $R[\Omega] \geq 0,02 \cdot v_{DM}[V]$
 $C \leq 0,33\mu F$

Steuergenerator /
 Pulse generator:
 $i_G = 1A$
 $di_G/dt = 1A/\mu s$

EDP-Diagramm /EDP-diagram
 Gesamtenergie W_{tot} je Durchlaßstromplus /
 Total energy W_{tot} per on-state current pulse

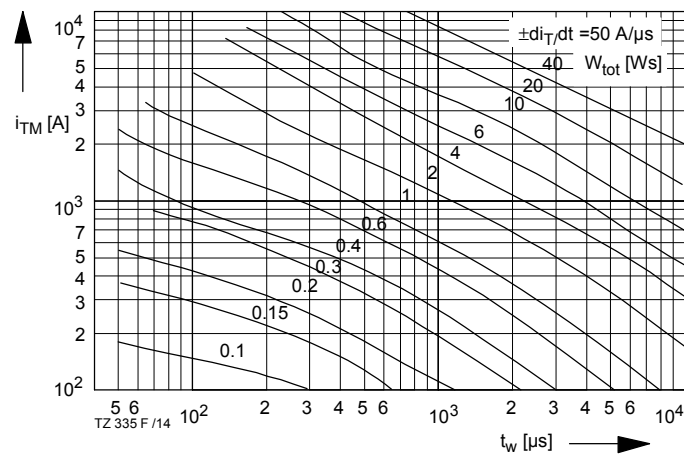
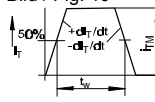
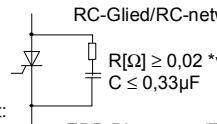


Bild / Fig. 10



Lastkreis / Load circuit:
 $v_{DM} \leq 67\% V_{DRM}$
 $v_{RM} \leq 67\% V_{RRM}$
 $dv_R/dt \leq 600V/\mu s$



RC-Glied/RC-network:
 $R[\Omega] \geq 0,02 \cdot v_{DM}[V]$
 $C \leq 0,33\mu F$

Steuergenerator /
 Pulse generator:
 $i_G = 1A$
 $di_G/dt = 1A/\mu s$

EDP-Diagramm /EDP-diagram
 Gesamtenergie W_{tot} je Durchlaßstromplus /
 Total energy W_{tot} per on-state current pulse

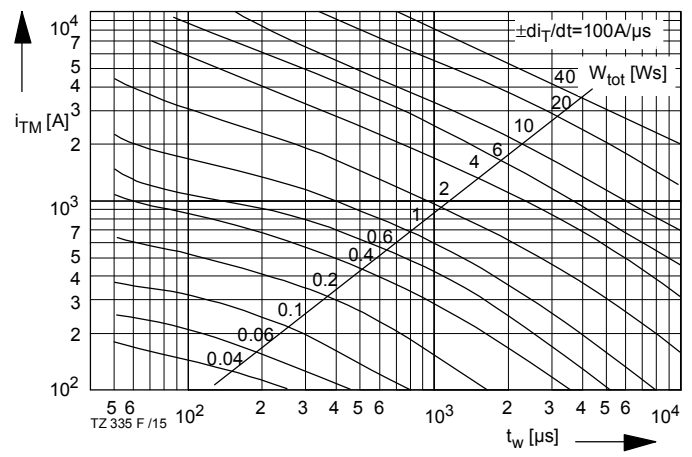
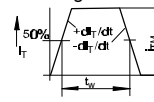
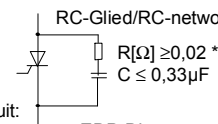


Bild / Fig. 11



Lastkreis / Load circuit:
 $v_{DM} \leq 67\% V_{DRM}$
 $v_{RM} \leq 50V$
 $dv_R/dt \leq 100V/\mu s$



RC-Glied/RC-network:
 $R[\Omega] \geq 0,02 \cdot v_{DM}[V]$
 $C \leq 0,33\mu F$

Steuergenerator /
 Pulse generator:
 $i_G = 1A$
 $di_G/dt = 1A/\mu s$

EDP-Diagramm /EDP-diagram
 Gesamtenergie W_{tot} je Durchlaßstromplus /
 Total energy W_{tot} per on-state current pulse

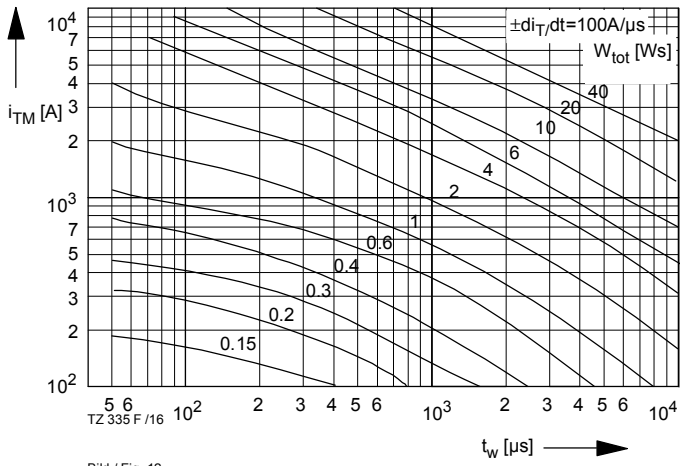
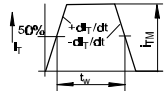
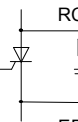


Bild / Fig. 12



Lastkreis / Load circuit:
 $v_{DM} \leq 67\% V_{DRM}$
 $v_{RM} \leq 67\% V_{RRM}$
 $dv_R/dt \leq 600V/\mu s$



RC-Glied/RC-network: Steuergenerator / Pulse generator:
 $R[\Omega] \geq 0,02 \cdot v_{DM}[V]$ $i_G = 1A$
 $C \leq 0,33\mu F$ $di_G/dt = 1A/\mu s$

EDP-Diagramm / EDP-diagram
 Gesamtenergie W_{tot} je Durchlaßstromplus /
 Total energy W_{tot} per on-state current pulse